AN200498

Enabling S25FL128S and S25FL127S to Configure Altera® Cyclone® V

AN200498 shows how to enable Cypress S25FL128S and S25FL127S SPI flash for configuring the Cyclone V under Active Serial (AS) mode.

1 Introduction

Altera® provides various methods to configure their Cyclone® series Field-Programmable Gate Array (FPGA). Every time the part is powered up, the configuration data is loaded in volatile RAM from some external source.

The Cyclone V E FPGA is capable of being configured from SPI flash, Parallel NOR flash, or JTAG. When configuring the FPGA with SPI flash, customers generally have no other choice but to use either Altera EPCS® or EPCQ® flash as the configuration device.

This application note shows how to enable Cypress S25FL128S and S25FL127S SPI flash for configuring the Cyclone V under Active Serial (AS) mode.

2 Required materials

All techniques demonstrated in this application note are tested on an Altera Cyclone V E FPGA Development Board with the following FPGA part number: 5CEFA7F31I7N. The sample design is built by using the Altera Quartus® II Web Edition version 14.0.

- Altera Cyclone V E FPGA Development Board
  - http://www.altera.com/products/devkits/altera/kit-cyclone-v-e.html
- Altera Quartus® II Subscription Edition or Web Edition version 14.0
  - http://www.altera.com/products/software/sfw-index.jsp
- Cypress S25FL128S (demonstrated here) or S25FL127S
  - http://www.cypress.com/documentation/datasheets/s25fl256s-256-mbit-30v-spi-flash-memory-datasheet

Note: When the older version of Quartus® II is used, the Cyclone V cannot be configured with Cypress FL-S via the procedure described here. Quartus II version 14.0 is required for the procedure described here; it is expected that later versions of Quartus II will also work.

Note: The Cyclone V cannot be configured with other Cypress larger density FL-S parts over 128 Mb due to differences of the 4-byte addressing scheme between Altera and Cypress devices.

3 Procedures

1. Change the Latency Code (LC) of the Configuration Register (CR1) on Cypress S25FL128S device.

   Table 1 lists the internal clock frequency specification for the AS configuration scheme on Cyclone V. In the procedure described here, the Cyclone V device is configured at the clock frequency of maximum 100 MHz.

   To enable any read command on Cypress S25FL128S at less than 100 MHz, the LC bits of CR1 are programmed with 0b10 in advance. Refer to Table 2 for CR1 and Table 3 for LC bit setting.

LC of CR1 is programmed with the Write Registers (WRR) command. Refer to the Cypress S25FL128S datasheet.

Table 1. Clock Frequency Specification in the AS Configuration Scheme for Cyclone V

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

Table 2. Configuration Register 1 (CR1)

Bits	Field Name	Function	Type	Default State	Description
7	LC1	Latency Code	Non-Volatile	0	Select number of initial read latency cycles. See Table 3.
6	LC0			0	
5	TBPROT	Configures Start of Block Protection	OTP	0	1 = BP starts at bottom (Low address) 0 = BP starts at top (High address)
4	RFU	RFU	OTP	0	Reserved for future use
3	BPNV	Configures BP2-0 in Status Register	OTP	0	1 = Volatile 0 = Non-Volatile
2	TBPARM	Configures Parameter Sectors location	OTP	0	1 = 4-KB physical sectors at top (high address) 0 = 4-KB physical sectors at bottom (low address) RFU in uniform sectors devices
1	QUAD	Puts the device into Quad I/O operation	Non-Volatile	0	1 = QUAD 0 = Dual or Serial
0	FREEZE	Lock current state of BP2-0 bits in Status Register, TBPROT and TBPARM in Configuration Register, and OTP regions	Volatile	0	1 = Block Protection and OTP locked 0 = Block Protection and OTP un-locked

Table 3. Latency Code Table

Freq. (MHz)	LC	Read (03h, 13h)		Fast Read (0Bh, 0Ch)		Read Quad Out (6Bh, 6Ch)		Quad I/O Read (EBh, ECh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	0	0	0	0	0	4	2	1
≤ 80	00	—	—	0	8	0	4	2	4
≤ 90	01	—	—	0	8	0	5	2	4
≤ 104	10	—	—	0	8	0	6	2	5
≤ 133	10	—	—	0	8	—	—	—	—

2. Enable Active Serial (AS) mode.
   a. Normally Fast Passive Parallel (FPP) mode is enabled on the Cyclone V E development board. To configure the FPGA to AS mode, remove R16 and R23 resisters and add R18 and R23 resisters.
   b. There are four dip switches on the board. For the AS mode configuration, SW1, SW2, and SW3 settings must be set as shown in Table 4.

Table 4. SW1, SW2 and SW4 Dip Switch Settings for AS Mode Available

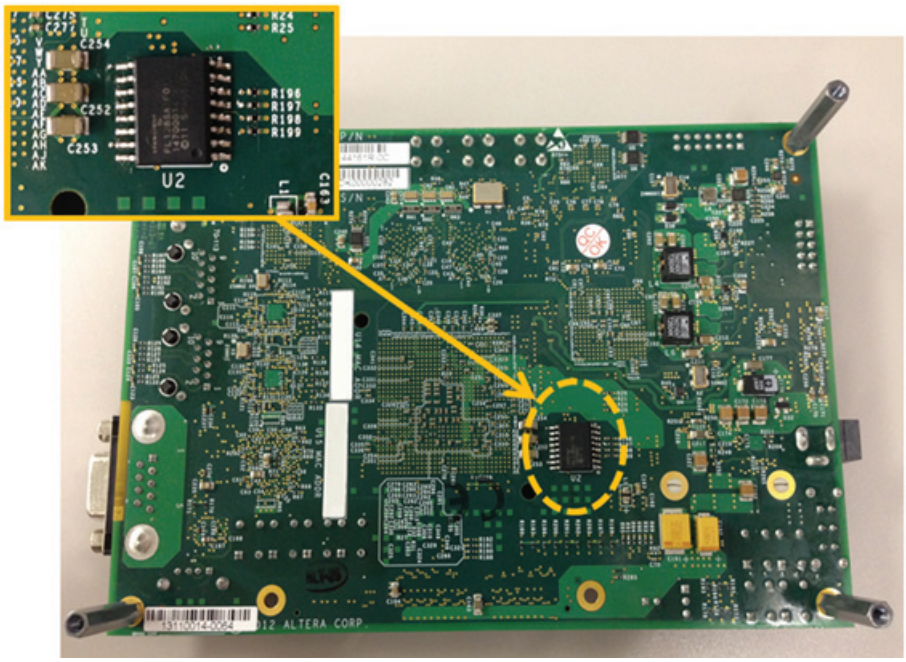
Switch	Board Label	Position
SW1	FPGA_MSEL 0	OFF
	FPGA_MSEL 1	OFF
	FPGA_MSEL 2	ON
	FPGA_MSEL 4	OFF
SW2	FAN_FORCE_ON	OFF
	HSMA_JTAG_EN	ON
	5M2210_JTAG_EN	OFF
	Reserved	OFF
SW4	CLK_SEL	ON
	CLK_EN	OFF
	FAC_LOAD	OFF
	SECURITY	OFF

Note: To proceed to the next step, AS configuration must be enabled on the board. You can download your design into the Altera EPCQ on the board to check if the FPGA configuration works correctly under the AS mode.

3. Replace Altera EPCQ with Cypress S25FL128S.

   The EPCQ device is placed at the bottom side of the board. Figure 1 shows the Cypress S25FL128S mounted in place of the EPCQ.

Figure 1. Bottom Side View of the Altera Cyclone V E FPGA Development Board with Cypress S25FL128S Soldered In Place



4. Create a .sof file for your design.

a. Create your Quartus II project and design.

b. Run 'Device' from the Quartus II Assignments menu.

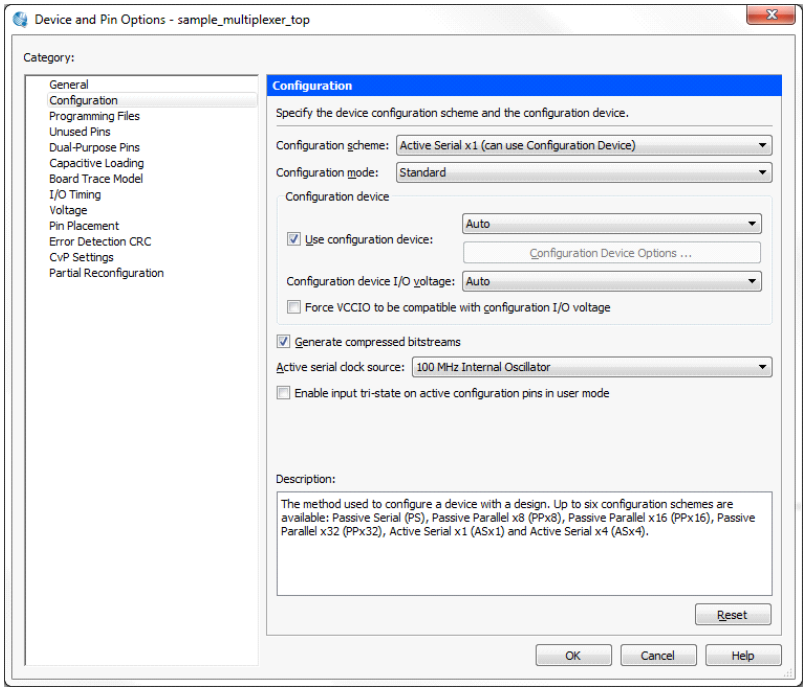
c. Click the 'Device and Pin Options…' button.

d. Select the 'Configuration' as the 'Category'.

e. Select the 'Active Serial x1' as the 'Configuration scheme'.

f. Select the '100 MHz Internal Oscillator' as the 'Active serial clock source'.

g. Click the 'OK' button to close.



5. Create a customized quartus.ini file.

   When selecting SPI flash for the Cyclone V configuration, customers generally have only two options either Altera EPCS or EPCQ flash on the Quartus II.

   To get the Cypress S25FL128S to be selected on the Quartus II, create a customized quartus.ini file in the project directory. Contact Altera support to get the contents of the file that can work for your design at the following web page: https://www.altera.com/about/contact/technical-support.html.

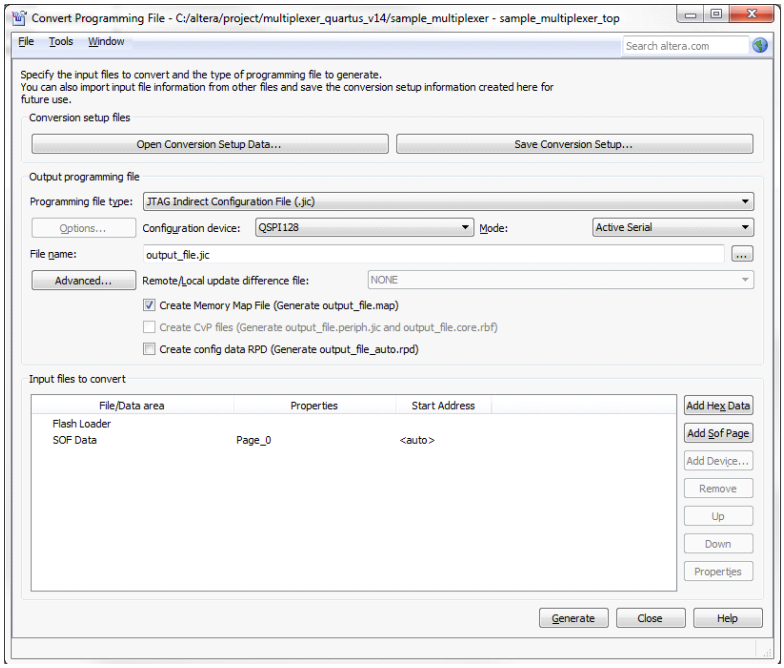
6. Generate ‘Programmer Object File’ (.POF) or ‘JTAG Indirect Configuration File’ (.JIC) for Cypress S25FL128S.

   a. Run 'Convert Programming File' from the Quartus II File menu.

   b. Select ‘JTAG Indirect Configuration File’ (.JIC) as the 'Programming file type' here. The ‘Programmer Object File’ (.POF) is also valid for Cypress S25FL128S and S25FL127S.

   c. Select 'QSPI128' as the 'Configuration device'.

   d. Select 'Active Serial' or 'Active Serial x4' as the 'Mode'.



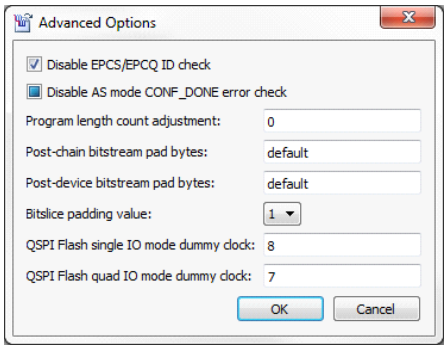
e. Click the 'Advanced…' button.

f. Check off the 'Disable EPCS ID check'.

g. Assign the 'QSPI Flash single IO mode dummy clock' with 8. As described at Step 1. and Step 4.a-f, the Cyclone V device is configured at less than 100 MHz clock rate and the LC bits of CR1 on Cypress S25FL128S device are programmed with 0b10. So the number of the dummy clock becomes 8. Refer to Table 3.

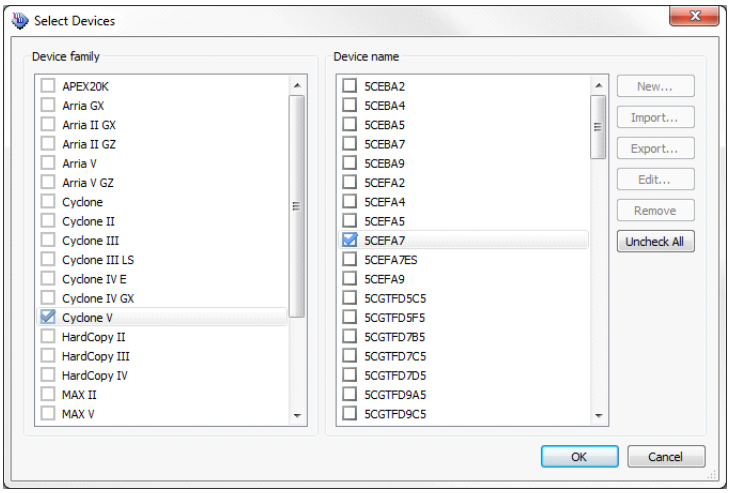
h. Assign the 'QSPI Flash quad IO mode dummy clock' with 7. As described at Step 1. and Step 4.a-f, the Cyclone V device is configured at less than 100 MHz clock rate and the LC bits of CR1 on Cypress S25FL128S device are programmed with 0b10. So the number of the dummy clock becomes 7. Refer to Table 3.

i. Click the 'OK' button to close.



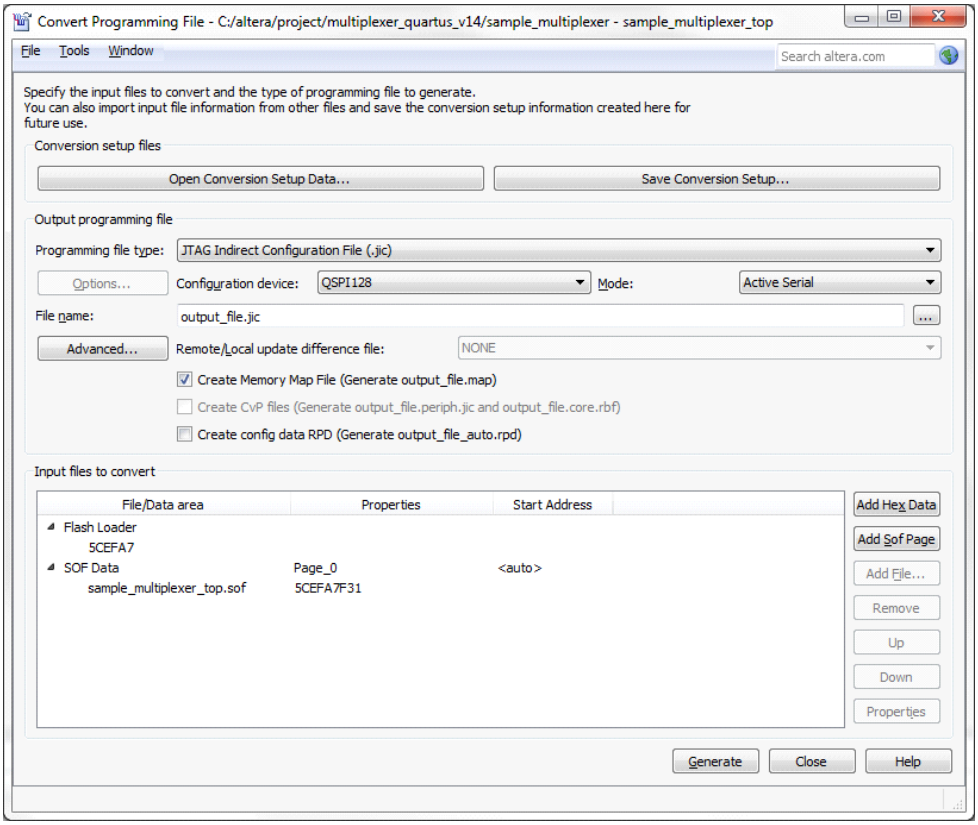
j. In the 'Input files to convert' window, click on the 'Flash Loader' line, then click 'Add Device…'.

k. Select the 'Cyclone V' as the 'Device family' and the '5CEFA7' as the 'Device name'.



l. Click on the 'SOF data' line, then click 'Add File'. Select your .sof file.

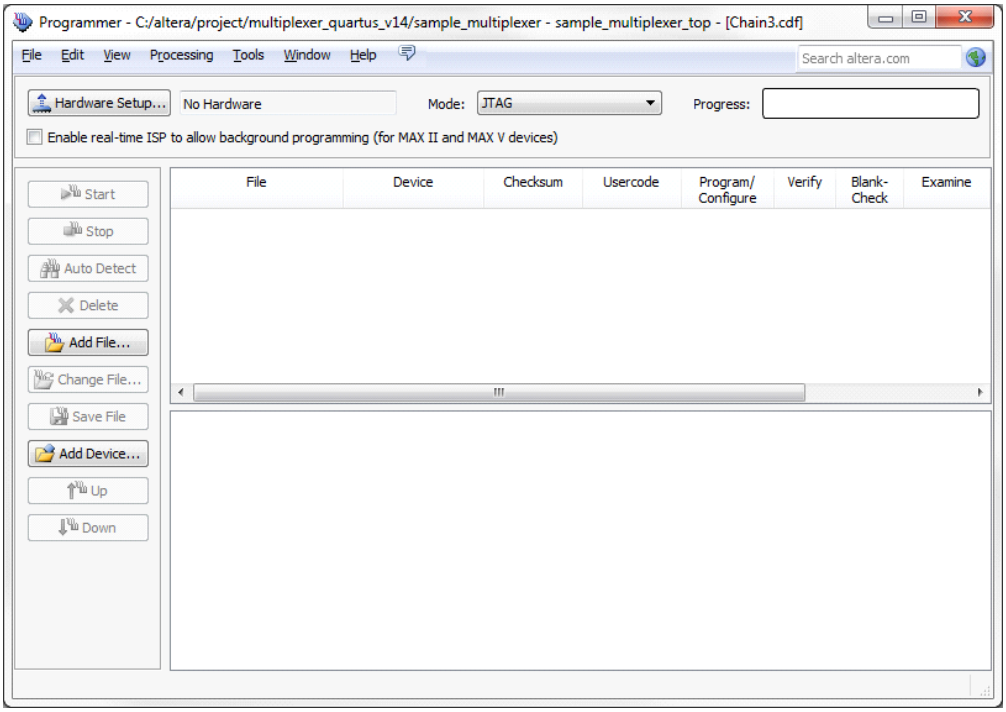
m. Click the 'Generate' button. And click the 'Close' button.



7. Program your design into the Cypress S25FL128S on the Cyclone V E development board.

   a. To program your design via the Altera on-board Byte Blaster®, connect the host PC with the board via the USB cable.

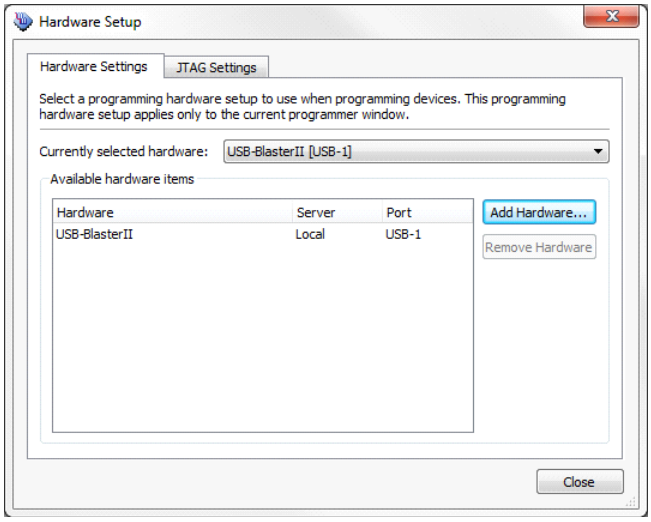
   b. Select the 'Programmer' from the Quartus II Tools menu.



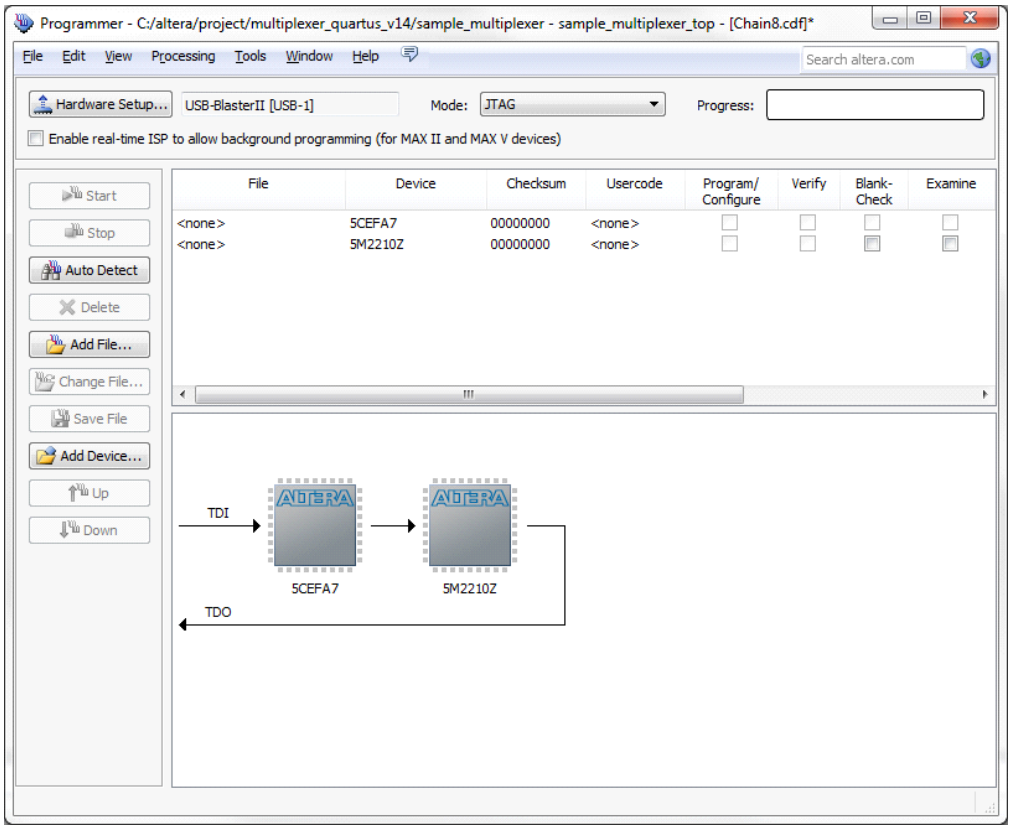
c. Click the 'Hardware Setup…' button.

d. Open the 'Hardware Settings' tab window. Select the 'USB-Blaster II' as the 'Currently selected hardware'.

e. Click the 'Close' button.



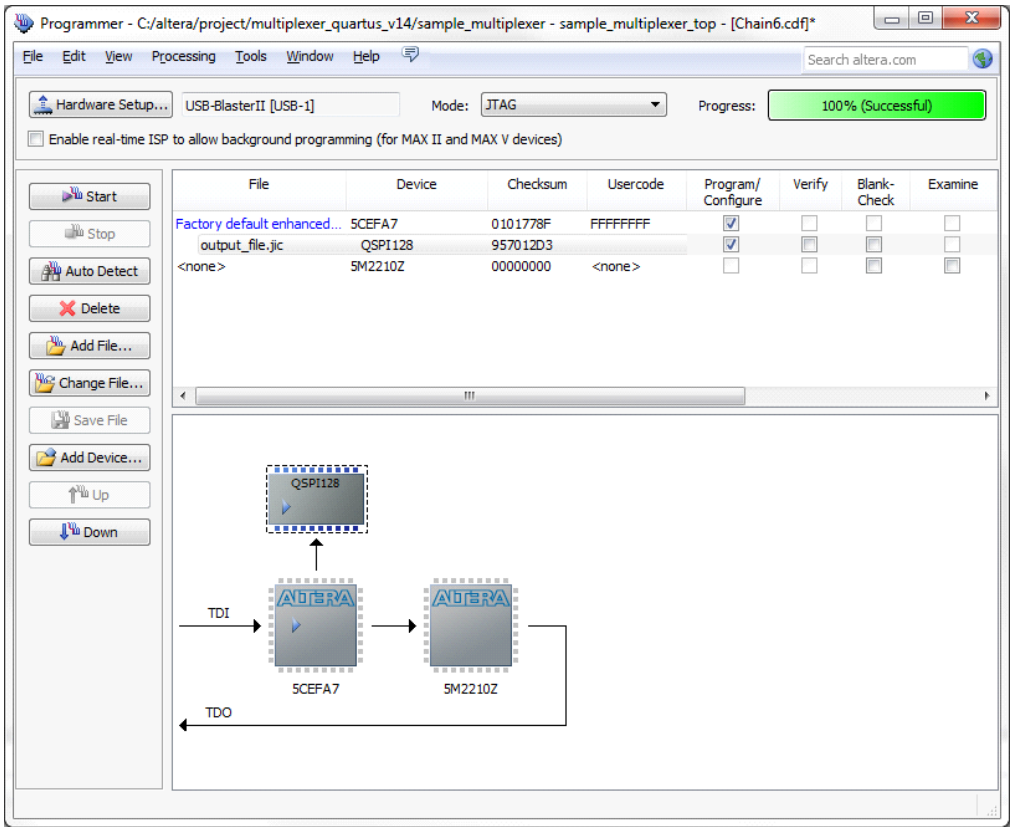
f. Click the 'Auto Detect' button to detect the Cyclone V device on the board. Then the 'Programmer' window will be updated with the list of Altera Cyclone V 5CEFA7 part and Altera MAX® V FPGA.



g. Click on the File field at the '5CEFA7' device line. And open your .jic file generated at Step 6. Then the 'QSPI128' device will appear with the list of the Cyclone V and MAX V FPGA parts.

h. Check off the 'Program/Configure' button at the 'QSPI128' device line.

i. Click the 'Start' button to download your design into Cypress FL128S. You will see '100%(Successful)' after the download is complete. After that, reboot the board to verify that your design runs on the Cyclone V configured from Cypress S25FL128S.



4 Conclusion

This application note teaches the seven steps to enable Cypress S25FL128S on the Altera Cyclone V E development board as the configuration device. This method also works for Cypress S25FL127S, and can be extended to other Cyclone V FPGA board designs.

5 References

- Altera Cyclone V E FPGA Development Kit - User Guide ver1.1
  - http://www.altera.com/literature/ug/ug_cve_fpga_dev_kit.pdf
- Altera Cyclone V E FPGA Development Kit - Kit installation ver12.1.1.0
  - https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-cyclone-v-e.html
- Cyclone V Device Data sheet
  - http://www.altera.com/literature/hb/cyclone-v/cv_51002.pdf
- Cyclone V Device Handbook: Chapter 7 - Configuration, Design Security, and Remote System Upgrades in Cyclone V Devices
  - http://www.altera.com/literature/hb/cyclone-v/cv_52007.pdf
- Cypress S25FL127S and S25FL128S datasheet
  - http://www.cypress.com/documentation/datasheets/s25fl256s-256-mbit-30v-spi-flash-memory-datasheet

Document History Page

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**	–	–	11/25/2014	Initial version
*A	5139192	MSWI	02/16/2016	Updated in Cypress template
*B	5179256	NOHA	05/25/2016	Updated Step 5 of Section 3 Procedures

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